forming a multilayer insulating film comprising at least two layer over said gate region and over said source-drain regions; and

forming holes in said multilayer insulating film by dry etching techniques so as to form tapered sections having tilt angles which decrease successively from said top insulating layer toward said bottom insulating layer of the film]

A1 Contd

A semiconductor device comprising:

a semiconductor layer having at least channel, source and drain regions;

an insulating film formed on said semiconductor layer;

C1 Cont

a first interlayer insulating film over said insulating film;

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising a different material from said insulating film;

a first opening in said insulating film for exposing a portion of said semiconductor layer;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said insulating film where surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor layer, said

portion of said insulating film and a portion of said first interlayer insulating film where surrounds said second opening, wherein edges of at least said first and third openings are rounded off.

Please add the following new claims.

2. (New) A device according to claim 1 wherein a taper angle β of the second interlayer insulating film with respect to said semiconductor layer in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to said semiconductor layer in the second opening.

3. (New) A device according to claim 1, wherein said insulating film comprises silicon oxide.

4. (New) A device according to claim 1, wherein said first and second interlayer insulating films comprise a material selected from the group consisting of silicon nitride and organic resin.

5. (New) A device according to claim 1, wherein said second interlayer insulating film has a dry etching rate higher than said first interlayer insulating film.

A2 cont'd

6. (New) A semiconductor device comprising:

Sub B1

a semiconductor layer formed over a substrate having an insulating surface, said semiconductor layer having at least channel, source and drain regions;

a gate insulating film over a semiconductor layer;

a first interlayer insulating film over said gate insulating layer;

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising a different material from said gate insulating film;

a first opening in said gate insulating film for exposing a portion of said semiconductor layer;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said gate insulating film where surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor layer, said

portion of said gate insulating film and a portion of said first interlayer insulating film where surrounds said second opening,

wherein edges of at least said first and third openings are rounded off, and

wherein a taper angle β of the second interlayer insulating film with respect to said semiconductor layer in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to said semiconductor layer in the second opening.

7. (New) A device according to claim 6, wherein said gate insulating film comprises silicon oxide.

8. (New) A device according to claim 6, wherein said first and second interlayer insulating film comprise a material selected from the group consisting of silicon nitride and organic resin.

9. (New) A device according to claim 6, wherein said second interlayer insulating film has a dry etching rate higher than said first interlayer insulating film.

10. (New) A semiconductor device comprising:

a semiconductor layer having at least channel, source and drain regions;

an insulating film on said semiconductor layer

a first interlayer insulating film over said insulating film;

a second interlayer insulating film on said first interlayer insulating film;

a first opening in said insulating film for exposing a portion of said semiconductor layer;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said insulating film where surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor layer, said portion of said insulating film and a portion of said first interlayer insulating film where surrounds said second opening,

wherein a taper angle β of the second interlayer insulating film with respect to said semiconductor layer in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to said semiconductor layer in the second opening.

C3 cont.

11. (New) A device according to claim 10, wherein said gate insulating film comprises silicon oxide.

C7 cont'd

12. (New) A device according to claim 10, wherein said first and second interlayer insulating film comprise a material selected from the group consisting of silicon nitride and organic resin.

13. (New) A device according to claim 10, wherein said second interlayer insulating film has a dry etching rate higher than said first interlayer insulating film.

14. (New) A semiconductor device comprising:

a semiconductor layer including at least channel, source and drain regions;

an insulating film on said semiconductor layer

C4

multi-interlayer insulating films comprising at least an upper insulating layer and a lower insulating layer over said insulating film, said lower insulating layer comprising the same material as said upper insulating layer; and

at least one contact hole in said multi-interlayer insulating films and said insulating film, said contact hole having a tapered section,

wherein a taper angle β of an inner surface of the upper insulating layer in the contact hole with respect to a major surface of said semiconductor layer is larger than a taper angle α of an inner surface of the lower insulating layer in the contact hole with respect to said major surface of said semiconductor layer.

15. (New) A device according to claim 14, wherein said insulating film comprises silicon oxide.

16. (New) A device according to claim 14, wherein said first and second interlayer insulating films comprise a material selected from the group consisting of silicon nitride and organic resin.

17. (New) A device according to claim 14, wherein said upper insulating layer of said multilayer insulating films has a dry etching rate higher than said lower insulating layer.

18. (New) A device according to claim 14, wherein angles of the tapered section of the contact hole decrease successively from a top interlayer insulating layer toward a bottom interlayer insulating layer.

19. (New) A semiconductor device comprising:

a semiconductor layer having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor layer;

an interlayer insulating film consisting of a plurality of insulating layers over said semiconductor layer and said first interlayer insulating film; and

a contact hole in said interlayer insulating film and said insulating film for exposing a portion of said high doped impurity region, said contact hole has a tapered section,

wherein edges of said insulating film and said interlayer insulating film in said contact hole are rounded off, and

wherein angles of the tapered section of the contact hole decrease successively from a top interlayer insulating layer toward a bottom interlayer insulating layer.

20. (New) A device according to claim 19 wherein said insulating film comprises silicon oxide.

21. (New) A device according to claim 19 wherein at least one of said plurality of insulating layers in said interlayer insulating layer comprises a material selected from the group consisting of silicon nitride and organic resin.

22. (New) A device according to claim 19 wherein said low doped impurity region includes phosphorus at a dose of 0.1 to 5 x 10^{14} atoms/cm^2.

23. (New) A device according to claim 19 wherein said high doped impurity region includes phosphorus at a dose of 0.2 to 5 x 10^{15} atoms/cm^2.

24. (New) A semiconductor device comprising:

a semiconductor layer having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor layer;

an interlayer insulating film consisting of a plurality of insulating layers over said semiconductor layer and said first interlayer insulating film; and

a contact hole in said interlayer insulating film and said insulating film for exposing a portion of said high doped impurity region, said contact hole has a tapered section,

wherein edges of said insulating film and said interlayer insulating film in said contact hole are rounded off, and

wherein said portion of said high doped impurity region is apart from a junction between said low and high doped impurity regions.

25. (New) A device according to claim 24, wherein a taper angle β of an inner surface of an upper interlayer insulating film in the contact hole with respect to a major surface of said semiconductor layer is larger than a taper angle α of an inner surface of an lower interlayer insulating film in the contact hole with respect to said major surface of said semiconductor layer.

26. (New) A device according to claim 24, wherein angles of the taper shape of the contact hole decrease successively from a top interlayer insulating layer toward a bottom interlayer insulating layer